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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
HARKNESS, CHARLES A

ART UNIT	PAPER NUMBER
2183	6

DATE MAILED: 08/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/941,142	WAH CHAN ET AL.
	Examiner	Art Unit
	Charles A Harkness	2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 August 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 8-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Papers Submitted

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Pre-amendment as received on 02/21/02; and Change of Address as received on 03/06/02; and Revoke Power of Attorney as received on 03/18/02; and Change of Address as received on 11/15/02.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

3. The applicant or their representatives are urged to review the specification and submit corrections for all mistakes of a grammatical, clerical, or typographical nature.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-6 and 8-19 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-18 of U.S. Patent No. 6,282,637 (herein referred to as '637). Although the conflicting claims are not identical, they are not

patentably distinct from each other because claims 1 and 2's limitations are disclosed by claim 1 of patent '637 and removing elements (identifying and determining means) and their functions is not a patentable change (See *In re Karlson*, 311 F.2d 581, 583, 136 USPQ 184, 189 (CCPA 1963) and *In re Kulhe*, 526 F.2d 553, 188 USPQ 7(CCPA 1975)). "A trap condition" as claimed by claim 2, is the same as a cancellation condition as taught in '637's claim 1. In reference to claim 10, it is inherent that '637's claim 1 would require control and address and data terminals to be able to operate the cancellation of the execution and be able to perform the read and write operations from the cache to be able to function properly.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-6 and 8-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Barlow U.S. Patent Number 5,168,564 (herein referred to as Barlow).

5. Referring to claims1 and 14 Barlow has taught a computer processor capable to execute a computer instruction which locks and then unlocks a computer resource,

the computer processor being operable to lock the resource in the course of execution of the instruction before the processor has determined whether the instruction is to be executed to completion or canceled (Barlow column 1 lines 50-61; the resource is locked during the read portion of the operation),

the processor unlocking the resource by the time the instruction processing by the processor is terminated (Barlow column 1 lines 50-61; the resource is unlocked when the write portion is complete),

the unlocking being performed whether or not the instruction is canceled (Barlow column 2 lines 54-64 column 8 lines 25-59; the resource is unlocked when the operation is canceled or executed).

6. Referring to claims 2 and 16 Barlow has taught wherein the instruction execution is pipelined, and the instruction is canceled if a trap condition occurs after the processor started processing the instruction (Barlow column 7 line 60-column 8 line 3, figure 4a, column 5 lines 9-18; the fault causes the cancel command, which is the same thing as a trap, or exception).

7. Referring to claims 3 and 17 Barlow has taught wherein executing the instruction comprises reading a first memory location and conditionally or unconditionally writing a second memory location (Barlow column 8 lines 5-25; the second and first memory location may be the same location); and

The resource comprises the second memory location to be written (column 8 lines 10-25; the resource locked is a specific memory location).

8. Referring to claims 4 and 18 Barlow has taught further comprising a cache wherein the cache corresponds to the resource and comprises the second memory location (Barlow column 5 lines 26-40, column 9 line 53-column 10 line 16).

9. Referring to claims 5 and 19 Barlow has taught wherein the processor is operable to perform the reading before the processor has determined whether the instruction is to be canceled

(Barlow column 2 lines 40-53, column 9 line 53-column 10 line 16; since the cancel command can be asynchronous, the cancel command can be issued anytime).

10. Referring to claim 6 Barlow has taught wherein in combination with another processor having access to the same resource (Barlow column 9 lines 3-26).

11. Referring to claim 8 Barlow has taught wherein each instruction is executed in a plurality of pipeline stages, wherein the pipeline stages for each instruction include a stage ST1 in which a signal is generated by the processor to indicated whether the instruction is to be canceled due to a trap (Barlow figure 4a column 2 lines 54-64, column 9 line 53-column 10 line 16); and

When executing the instruction which locks and then unlocks the computer resource, the processor is operable to lock the computer resource before the stage ST1 (Barlow figure 4a column 2 lines 54-64, column 9 line 53-column 10 line 16).

12. Referring to claim 9 Barlow has taught wherein for at least some instructions including the instruction that locks and then unlocks the computer resource, the stage ST1 is followed by a stage ST2 in which at least one instruction result is written to an architecture storage location (Barlow figure 4a column 2 lines 54-64, column 9 line 53-column 10 line 16); and

When the processor executes the instruction that locks and then unlocks the computer resource, and the instruction is to be canceled, the stage ST2 is executed for the instruction to unlock the resource but writing to the architecture storage location is suppressed (Barlow column 7 lines 53-59, column 14 lines 3-12).

13. Referring to claim 10 Barlow has taught a computer processor comprising an interface to a cache, the interface comprising:

Address and data terminals (Barlow column 5 lines 26-40, column 9 line 53-column 10 line 16, column 5 line 62-column 6 line13, column 2 lines 4-26; inherently the cache would require some control terminals or circuits, and would also require signals coming into the cache to request a specific address and signals coming out of the cache that transfer data to the processor); and

One or more control terminals to lock and unlock at least a portion of the cache, the one or more control terminals being operable to indicate that the cache is not to store data but to perform an unlock operation (Barlow column 7 lines 53-59, column 14 lines 3-12, column 1 lines 50-61, column 2 lines 54-64 column 8 lines 25-59).

14. Referring to claim 11 Barlow has taught wherein in combination with said cache, the cache being connected to the address and data terminals and to the one or more control terminals (Barlow column 5 line 62-column 6 line13, column 2 lines 4-26; inherently the cache would require some control terminals or circuits, and would also require signals coming into the cache to request a specific address and signals coming out of the cache that transfer data to the processor).

15. Referring to claim 12 Barlow has taught further comprising:

A second processor having data and address terminals and one or more control terminals, wherein said terminals of the second processor are connected to the cache (Barlow figure 1, column 4 lines 6-51, column 2 lines 29-39).

16. Referring to claim 13 Barlow has taught further comprising a memory and a circuit for caching data from the memory in the cache (Barlow column 5 line 62-column 6 line13, column 2 lines 4-26; a cache memory be definition takes data from a main or other memory to use at the

processor level, so that the data will be move available to the processor and can be accessed more easily, which would require some circuits to control the transfer of data).

17. Referring to claim 15 Barlow has taught wherein the unlocking is performed after the processor has determined whether the instruction is to be canceled (Barlow column 9 lines 20-41 column 8 line 59-column 9 line 2).

18. Referring to claim 20 Barlow has taught wherein the first memory location and the second memory location correspond to the same memory location (Barlow column 8 lines 10-25).

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR 1.111(c).

Stumpf et al, U.S. Patent Number 5,175,829 has taught a method and apparatus for bus lock during atomic computer operations.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 703-305-7579. The examiner can normally be reached on 8:00 A.M. – 5:30 P.M. with every other Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-7579.

Charles Allen Harkness

Examiner

Art Unit 2183

August 20, 2003

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